AMENDMENTS TO THE CLAIMS

Claims 1 – 18. (Cancelled)

19. (Currently amended) A dual damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

a second insulating layer provided over said metal layer;

a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer having a step coverage of about 100% and filled with a copper material;

a third insulating layer located over said second insulating layer;

a trench situated within said third insulating layer and extending to said via, said trench being lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material.

20. (Previously presented) The dual damascene structure of claim 19, wherein said second insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

21. (Previously presented) The dual damascene structure of claim 19, wherein said second insulating layer includes silicon dioxide.

22. (Previously presented) The dual damascene structure of claim 19, wherein said second insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

23. (Previously presented) The dual damascene structure of claim 19, wherein said third insulating layer includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

24. (Previously presented) The dual damascene structure of claim 19, wherein said third insulating layer includes silicon dioxide.

25. (Previously presented) The dual damascene structure of claim 19, wherein said third insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

26. (Original) The dual damascene structure of claim 19, wherein said titanium-silicon-nitride layer has a thickness of about 2,000 to 15,000 Angstroms.

27. (Original) The dual damascene structure of claim 19, wherein said titanium-silicon-nitride layer has a thickness of about 100 Angstroms.

28. (Original) The dual damascene structure of claim 19, wherein said copper material includes copper or a copper alloy.

29. (Cancelled)

30. (Previously presented) The dual damascene structure of claim 19, wherein said substrate is a silicon substrate.

31. (Currently amended) A damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS; and

at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer having a thickness of about 100 Angstroms and filled with a copper material.

32. (Cancelled)

33. (Previously presented) The damascene structure of claim 31, wherein said at least another insulating layer includes silicon dioxide.

34. (Previously presented) The damascene structure of claim 31, wherein said at least another insulating layer has a thickness of about 2,000 to 15,000 Angstroms.

35. (Cancelled)

36. (Cancelled)

37. (Original) The damascene structure of claim 31, wherein said copper material includes copper or a copper alloy.

38. (Cancelled)

39. (Previously presented) The damascene structure of claim 31, wherein said substrate is a silicon substrate.

40. (Currently amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure, said damascene structure comprising a metal layer provided within a first insulating layer formed over a substrate, at least another insulating layer provided over said metal layer, said first insulating layer and said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS, an etch stop layer provided between said first insulating layer and said at least another insulating layer, and at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with copper.

41. (Original) The processor-based system of claim 40, wherein said processor and said integrated circuit are integrated on same chip.

42. (New) A damascene structure comprising:

a first insulating layer provided over a semiconductor substrate;

a metal layer provided within said first insulating layer;

at least another insulating layer provided over said metal layer, said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS;

an etch stop layer provided over and in contact with said at least another insulating layer; and

at least one opening situated within said at least another insulating layer and said etch stop layer, and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material.